RX32SD22 Data Sheet

Document number：DS00003

32-Bit professional Motor MCU based on Arm®Cortex®-M0 Core

Version：V2.4

Features

- Core: Arm®Cortex®-M0 CPU， frequency up to 42 MHz
- Operating conditions:
  - V_{DD}, V_{DDA} voltage range: 2.5 V to 5.5 V
- Motor Engine
  - 1 x 3 channels PID
  - 1 x SQRT
  - 1 x SVPWM
  - 1 x DIV
- Memories
  - 32 KB Flash
  - 4 KB SRAM
  - Flash Erase and Write 10Kcycle@105°C
  - Flash Erase and Write 100Kcycle@85°C
- Reset and supply management
  - POR, PDR, and programmable voltage detector (PVD)
  - Low-power modes: sleep, hold
- Clock management
  - Internal 42MHz oscillator
  - Internal 32KHz oscillator
  - 40MHz crystal oscillator
- DMA controller
  - 2 x independent programmable channels
- Up to 22 x fast I/Os
  - 22/20 I/Os

TSSOP28 (9.7 × 4.4 mm)
TSSOP24 (7.8 × 4.4 mm)

- 1 x 1Msps 12-bit ADC
  - 15 x channels ADC input
  - Conversion range：0V to AVCC
- Operational amplifier
  - 3 x PGA(Programmable)
- 2 x Rail to rail comparator(CMP)
- 2 x Communication interfaces
  - 1 x I²C
  - 1 x UART
- Debug mode
  - Serial wire debug (SWD)
- 7 x timers
  - 1 x 16-bit 5-channel advanced motor control timer, with up to 5 x PWM channels, dead time generation and emergency stop
  - 1 x SysTick timer: 24-bit downcounter
  - 4 x 16-bit general timers
  - 1 x watchdog timers (independent)
- PN-type half bridge gate drivers
  - Operating voltage: 10V~28V
  - Built-in 5V/40mA LDO
- CRC calculation unit, 96-bit unique ID

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the RX32SD22 microcontrollers.

This document should be read in conjunction with the reference manual "RX32S11_Reference_Manual". The data sheet and reference manual are both available from the Rxtek website www.rxtek-icore.com.

2 Description

The RX32SD22 device is based on the Arm® Cortex®-M0 32-bit RISC core, They operate at a frequency of up to 42 MHz.

The Cortex-M0 core supports all the Arm single-precision data-processing instructions and all the data types.

The device embeds high-speed memories (32 Kbytes of flash memory, and 4 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to one APB bus, one AHB bus.

The device embeds motor engine, include 1 x 3 channels PID, 1 x SQRT, 1 x SVPWM, 1 x DIV.

The device embeds 1 x ADC(1 Msps), 2 x comparator(CMP), 3 x Programmable Operational amplifier(PGA), 1 x 16-bit advanced motor control timers, 4 x 16-bit general timers, PN-type half bridge gate drivers.

The device features rich communication interfaces such as:

- One I2C
- One UART

The device operates in the -40 to +105 °C temperature ranges from a 2.5 to 5.5 V power supply.

RX32SD22 device offers TSSOP28 package with 28-pin and TSSOP24 package with 24-pin.

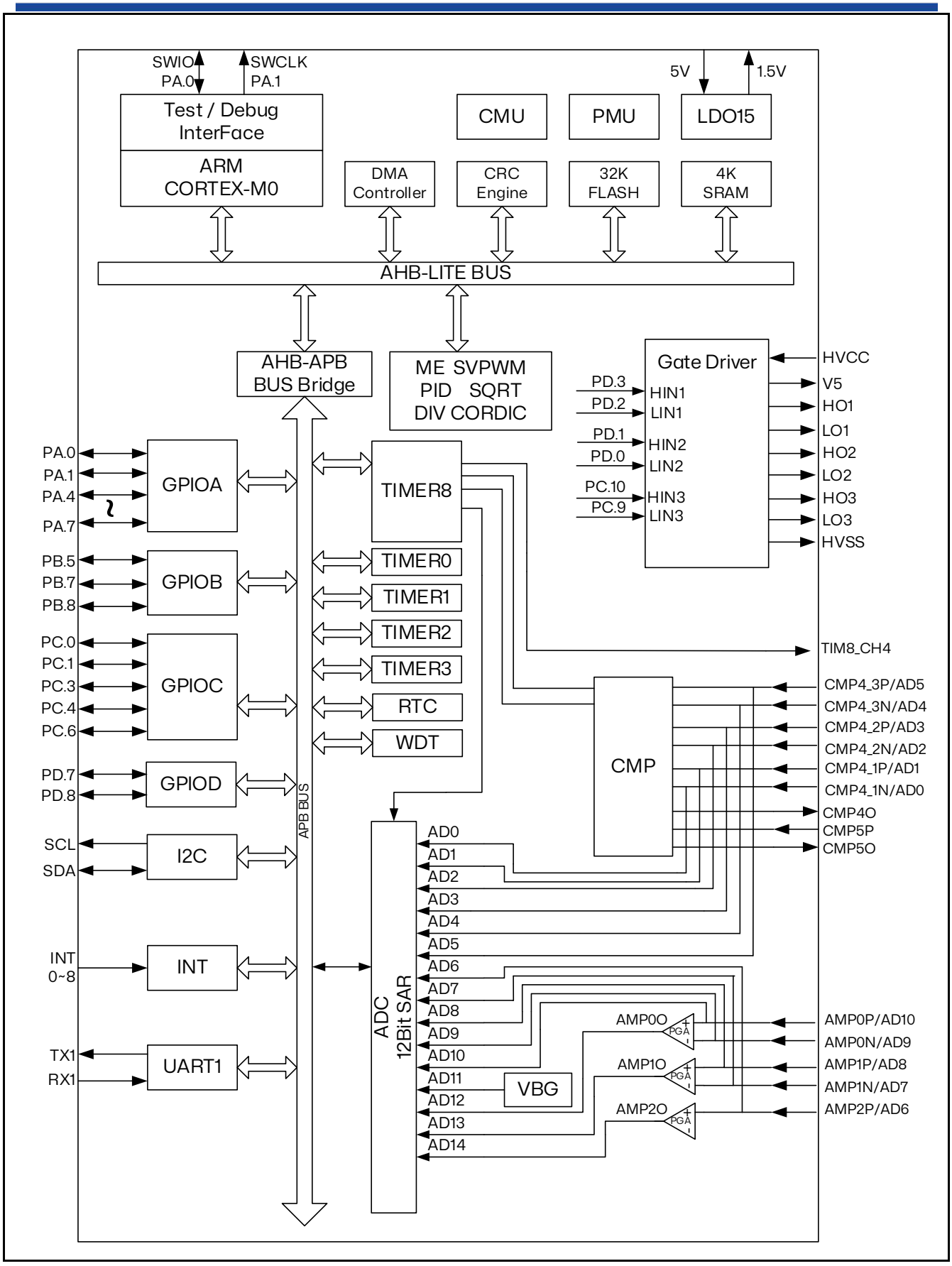


Figure 2.1 RX32SD22 Block diagram

3 Functional overview

3.1 Arm® Cortex®-M0 core

The Arm® Cortex®-M0 is a generation of Arm 32-bit RISC processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The Arm® Cortex®-M0 32-bit RISC processor features an exceptional code-efficiency.

3.2 Motor engine

The RX32SD22 provides a motor engine (ME), includes computation acceleration units for FOC operations:

- Clarke: Converts a 3-axis vector to an absolute coordinate vector(α-β)
- Park: Convert the absolute coordinate vector to the d-q axis vector
- RevPark: Reverts d-q axis vectors back to absolute coordinate vectors
- SVPWM: Computes 3-phase PWM output values from absolute coordinate vectors
- PID: Proportional-Integral-Derivative computation accelerator
- SQRT: Square root computation accelerator
- DIV: Division computation accelerator

3.3 Embedding Flash

RX32SD22 features 32 Kbytes of embedded Flash memory which is available for storing programs and data.

3.4 Embedding SRAM

The RX32SD22 features 4KB of SRAM. This SRAM can be accessed in byte (8-bit), half-word (16-bit), or word (32-bit) configurations without waiting cycles by the CPU or DMA.

3.5 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a configurable generator polynomial value and size. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

3.6 Power management

3.6.1 Power supply schemes

RX32SD22 device requires a 2.5V to 5.5V operating voltage supply.

3.6.2 Power on reset (POR) and power down reset (PDR)

RX32SD22 has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V.

The device remains in reset mode when V_{DD}/V_{DDA} is below a specified threshold, $V_{POR}/_{PDR}$, without the need for an external reset circuit. For details of power-on reset (POR)/power-down reset (PDR), please refer to the electrical characteristics section of the data sheet.

3.6.3 Low-power modes

RX32SD22 device supports two low-power modes, user can choose among the following modes:

- Sleep mode: In Sleep mode, the CPU is stopped and maintains the current state without any operations, while still being powered normally. When the user needs to achieve the lowest power consumption in this mode, user can turn off the high-power LDO(which is enabled by default). In this mode the CPU can be woken up by any interrupts.
- Hold mode: In hold mode, the CPU is stopped, LDO is turned off, and peripherals stop running. In this mode, the CPU can be woken up by interrupts or events.

Note: SDK Libraries V1.5 Low-power modes corresponds to this new version of Data Sheet, the old version of SDK Libraries V1.4 and the previous version correspond to the old version of Data Sheet.

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

3.8 Direct memory access controller (DMA)

The device embeds 1 DMA (Direct Memory Access Controller).
Direct memory access (DMA) is used in order to provide a high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps the CPU resources free for other operations.

This DMA controller has 2 channels in total, each one dedicated to manage memory access requests from one or more peripherals. Each controller has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 2 independently configurable channels(requests)
  - Each channel is connected to a dedicated hardware DMA request, a software trigger is also supported on each channel.
- Priorities between requests from channels of one DMA are both software programmable (4

levels: very high, high, medium, low.)

- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- 3 event flags (DMA block transfer, DMA transfer complete and DMA transfer error) in a single interrupt request
- Memory-to-memory transfer
- Peripheral-to-memory, memory-to-peripheral, and peripheral-to-peripheral transfers

3.9 Analog to digital converter (ADC)

The device embeds one analog-to-digital converter with the following features:

- 12-bit native resolution, with built-in calibration
- 1 Msps maximum conversion rate

3.10 PN-type Gate Driver

The device embeds one PN-type half bridge gate driver with the following features:

- P/N MOS three-phase half-bridge output
- Supply voltage range: 10V to 28V
- Independent inputs for high-side PMOS and low-side NMOS
- Gate output 10V to PMOS (VCC > 14V)
- Compatible with 3.3V, 5V logic inputs
- Built-in 5V / 40mA LDO

4 Pinouts and pin distributions

4.1 TSSOP28 pin distributions

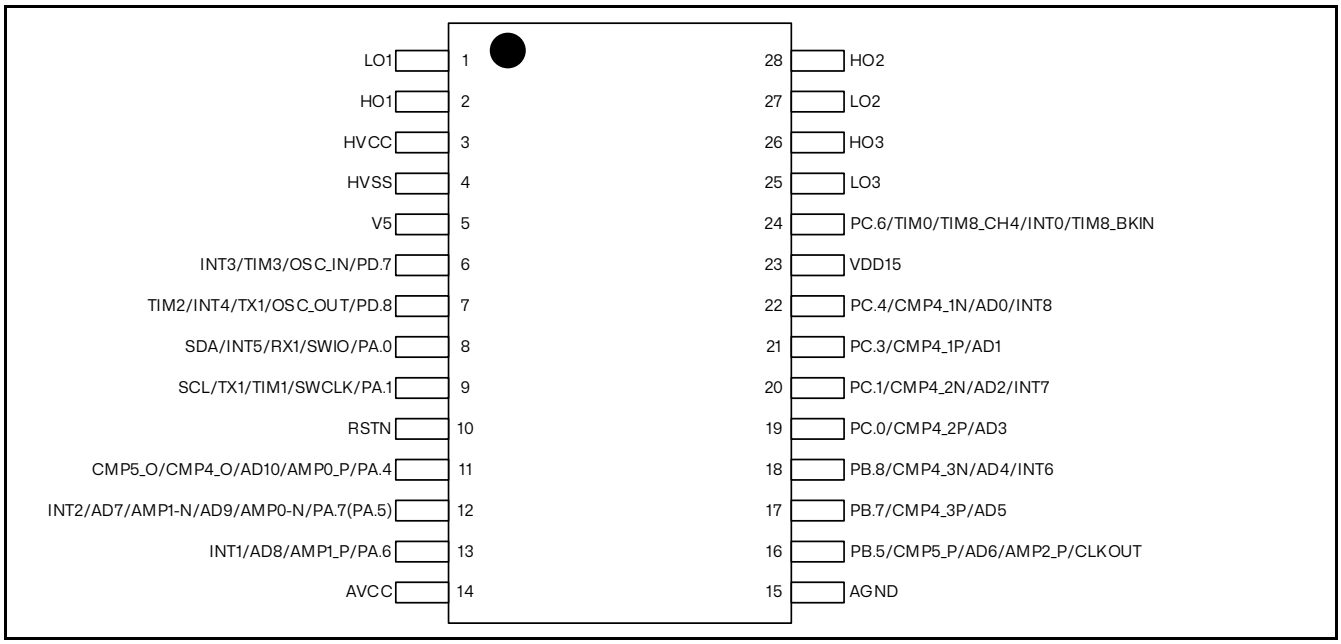


Figure 4.1 RX32SD22 TSSOP28 package pinout

4.2 TSSOP24 pin distributions

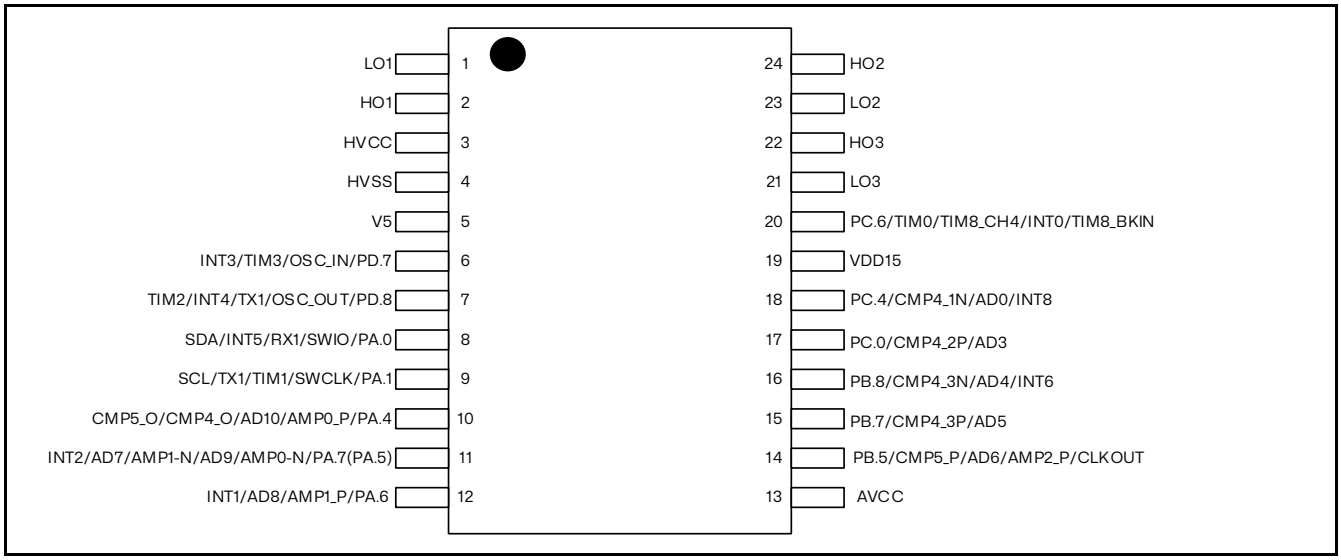


Figure 4.2 RX32SD22 TSSOP24 package pinout

4.3 Alternate function

Table 4.1 Alternate function (Port A)

Port		AF1	AF2	AF3	AF4
Port A	PA0	SWIO	RX1	INT5	SDA
	PA1	SWCLK	TIM1	TX1	SCL
	PA4	AMP0_P\AD10		CMP4_Out	CMP5_Out
	PA6	AMP1_P\AD8		INT1	
	PA7 (PA5)[1]	AMP1_N\AD7 AMP0_N\AD9		INT2	

1. AMP0_N\AD9 is the first alternate function of PA.5, and PA.5 is internally connected to PA.7.
When using the GPIO function of the PA.7 pin, please ensure that PA.5 is set to high-impedance state first to avoid interference.
When using other alternate functions, PA.5 can be directly set to high-impedance state.
When AD9 and AD7 are used simultaneously, they can only sample the same signal.
When AMP0_N and AMP1_N are used together, the N terminal of the amplifier can only be connected to the same signal.
It should be in high-impedance state when powered on.

Table 4.2 Alternate function (Port B)

Port		AF1	AF2	AF3	AF4
Port B	PB5	CMP5_P\AD6\AMP2_P			ClockOut
	PB7	CMP4_3P\AD5			
	PB8	CMP4_3N\AD4		INT6	

Table 4.3 Alternate function (Port C)

Port		AF1	AF2	AF3	AF4
Port C	PC0	CMP4_2P\AD3			
	PC1	CMP4_2N\AD2		INT7	
	PC3	CMP4_1P\AD1			
	PC4	CMP4_1N\AD0		INT8	
	PC6	TIM0	TIM8_CH4	INT0	TIM8_BKIN
	PC9(1)	TIM8_CH3N			
	PC10(1)	TIM8_CH3	TIM8_CH2N		

1. The pins have been sealed to the gate driver. Recommending alternate as Timer to use, otherwise it has no practical significance.

Table 4.4 Alternate function (Port D)

Port		AF1	AF2	AF3	AF4
Port D	PD0[1]	TIM8_CH2N	TIM8_CH1N		
	PD1[1]	TIM8_CH2	TIM8_CH3		
	PD2[1]	TIM8_CH1N	TIM8_CH2		
	PD3[1]	TIM8_CH1			
	PD7	OSC_IN	TIM3	INT3	
	PD8	OSC_OUT	TX1	INT4	TIM2

1. The pins have been sealed to the gate driver. Recommending alternate as Timer to use, otherwise it has no practical significance.

4.4 Pin definitions

Table 4.5 RX32SD22x6 pin definitions

Pins		Pin name (function after reset) (1)	Type (2)	Alternate functions
TSSOP24	TSSOP28			
1	1	LO1 (PD2) (3)	I/O	TIM8_CH1N, TIM8_CH2
2	2	HO1 (PD3) (3)	I/O	TIM8_CH1
3	3	HVCC(4)	P	-
4	4	HVSS	G	-
5	5	V5(4)	P	-
6	6	PD7-OSC_IN	I/O	OSC_IN, TIM3, INT3
7	7	PD8-OSC_OUT	I/O	OSC_OUT, TX1, INT4, TIM2
8	8	PA0 (SWIO)	I/O	SWIO, RX1, INT5, SDA
9	9	PA1 (SWCLK)	I/O	SWCLK, TIM1, TX1, SCL
-	10	RSTN	I	-
10	11	PA4	I/O	AMP0_P\AD10, CMP4_Out, CMP4_Out
11	12	PA7 (PA5) (5)	I/O	AMP1_N\AD7, INT2 (AMP0_N\AD9)
12	13	PA6	I/O	AMP1_P\AD8, INT1
13	14	AVCC(4)	P	-
-	15	AGND	G	-
14	16	PB5	I/O	CMP5_P\AD6\AMP2_P, ClockOut

Pins		Pin name (function after reset) (1)	Type (2)	Alternate functions
TSSOP24	TSSOP28			
15	17	PB7	I/O	CMP4_3P\AD5
16	18	PB8	I/O	CMP4_3N\AD4，INT6
17	19	PC0	I/O	CMP4_2P\AD3
-	20	PC1	I/O	CMP4_2N\AD2，INT7
-	21	PC3	I/O	CMP4_1P\AD1
18	22	PC4	I/O	CMP4_1N\AD0，INT8
19	23	VDD15	P	-
20	24	PC6	I/O	TIM0，TIM8_CH4，INT0，TIM8_BKIN
21	25	LO3 (PC9) (3)	I/O	TIM8_CH3N
22	26	HO3 (PC10) (3)	I/O	TIM8_CH3，TIM8_CH2N
23	27	LO2 (PD0) (3)	I/O	TIM8_CH2N，TIM8_CH1N
24	28	HO2 (PD1) (3)	I/O	TIM8_CH2，TIM8_CH3

1. Function availability depends on the chosen device.
2. I = input, O = output, P = Power, G = GND
3. The pins have been sealed to the gate driver. Recommending alternate as Timer to use, otherwise it has no practical significance.
4. Pin 3 (HVCC) of the TSSOP28 package, when powered, outputs through a built-in 5V/40mA LDO in the gate driver to pin 5 (V5). Since pin 5 (V5) is internally connected to AVCC and VCC, the microcontroller can operate directly without the need for an external LDO. However, in the TSSOP24 package, pin 5 (V5) is not internally connected to AVCC and VCC. Therefore, additional wiring is required to connect pin 5 (V5) to AVCC, or a separate LDO must be used to power AVCC for the microcontroller to function properly.
5. AMP0_N\AD9 is the first alternate function of PA.5, and PA.5 is internally connected to PA.7.
   When using the GPIO function of the PA.7 pin, please ensure that PA.5 is set to high-impedance state first to avoid interference.
   When using other alternate functions, PA.5 can be directly set to high-impedance state.
   When AD9 and AD7 are used simultaneously, they can only sample the same signal.
   When AMP0_N and AMP1_N are used together, the N terminal of the amplifier can only be connected to the same signal.
   It should be in high-impedance state when powered on.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 5.1.

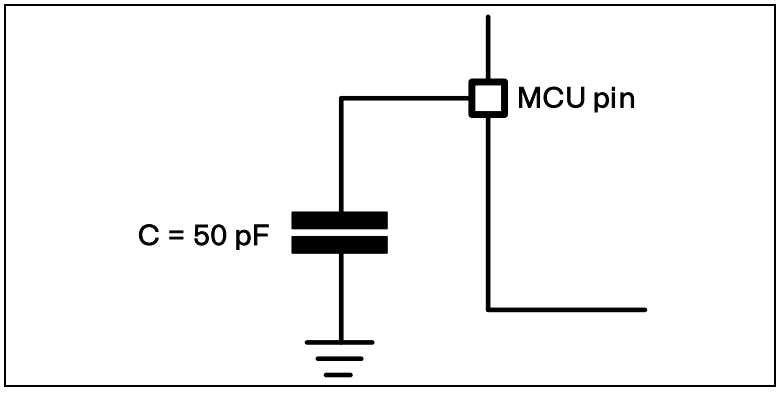


Figure 5.1 Pin loading conditions

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 5.2.

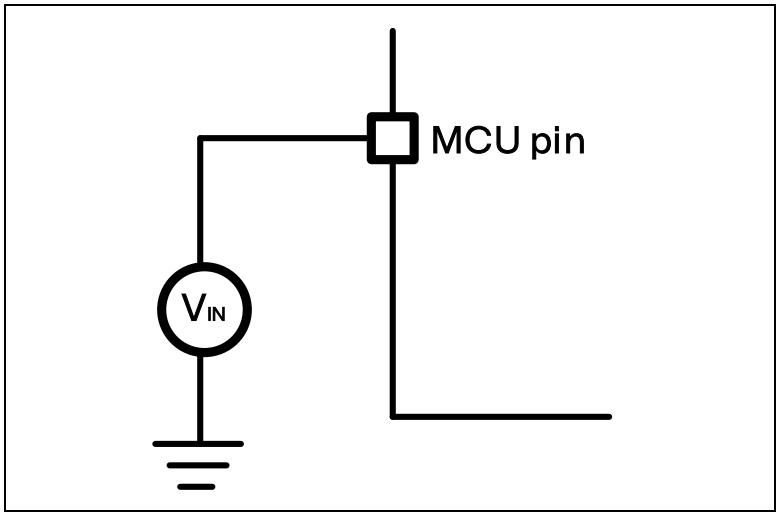


Figure 5.2 Pin input voltage

5.1.6 Power supply scheme

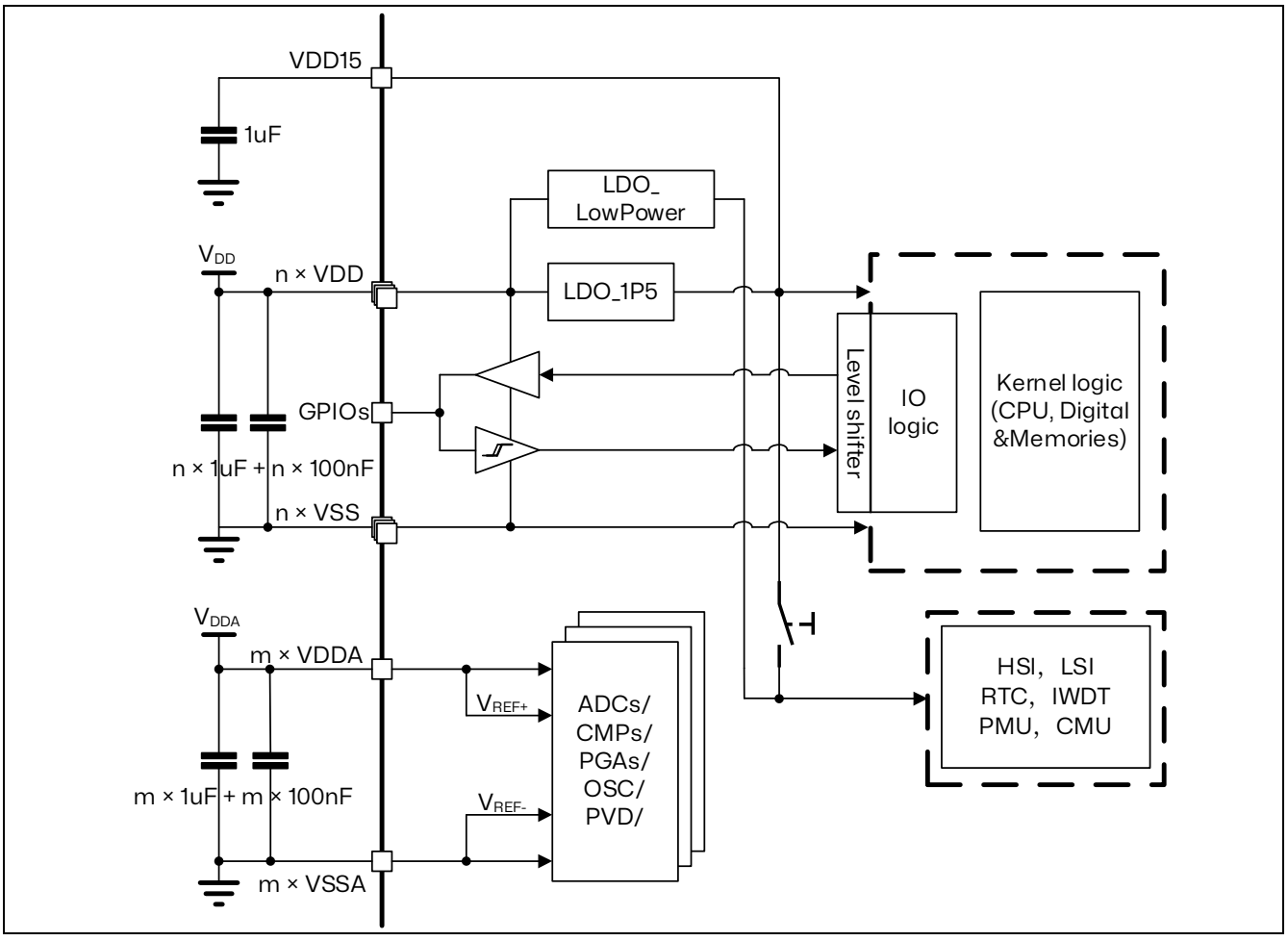


Figure 5.3 Power supply scheme

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

5.1.7 Current consumption measurement

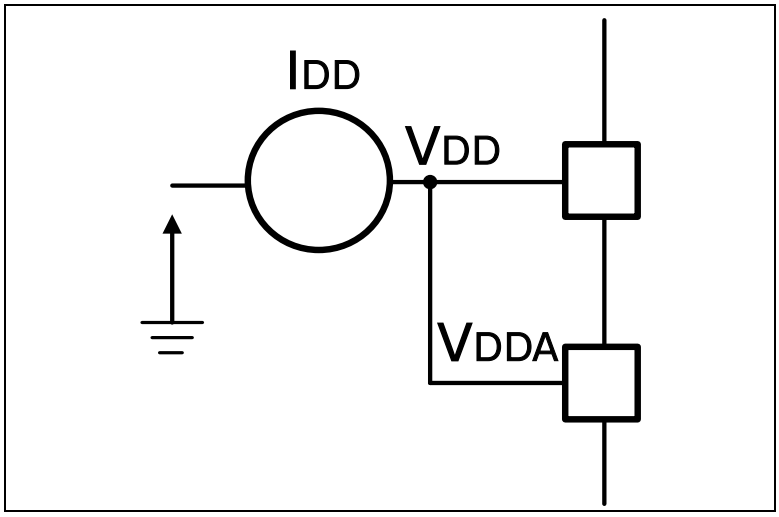


Figure 5.4 Current consumption measurement scheme

5.2 Absolute maximum ratings

The stresses loaded on the device may cause permanent damage to the device if it above the value given in "Absolute maximum ratings" in this section. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 5.1 Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD} - V_{SS}	External main supply voltage (include V_{DDA} and V_{DD}) (1)	-1	6.5	V
V_{IN}(2)	Input voltage on any other pin	-0.1V_{DD}	1.1V_{DD}	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between all the different ground pins	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	2		KV

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. VIN maximum must always be respected. Refer to Current characteristics for the maximum allowed injected current values.

Table 5.2 Current characteristics

Symbol	Ratings	Condition	Max	Unit
I_{VDD}	Total current into sum of all V_{DD}/V_{DDA} power lines (current of supply) (1)	VCC=3.3V	150	mA
		VCC=5V	150	

Symbol	Ratings	Condition	Max	Unit
I_{VSS}	Total current out of sum of all VSS ground lines (current of outflow)(1)	VCC=3.3V	50	
		VCC=5V	50	
I_{IO}	Total output current sunk by sum of all I/Os and control pins	VCC=3.3V	15	
		VCC=5V	15	
	Total output current sourced by sum of all I/Os and control pins	VCC=3.3V	15	
		VCC=5V	15	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. Negative injection disturbs the analog performance of the device.
3. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to Table 5.1 Voltage characteristics for the maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$.
5. When several inputs are submitted to a current injection, the maximum ΣIINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 5.3 Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 5.4 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	42	MHz
V_{DD}(1)	Standard operating voltage	-	2.5	5.5	V
V_{DDA}(1)	Analog operating voltage (use ADC or PGA or CMP)	Must have a potential equal to VDD(1)	2.5	5.5	
T_A	Ambient temperature	Maximum/low power dissipation	-40	105	°C
T_J	Junction temperature range		-40	150	

1. Refer to ADC characteristics for the ADC is used.
2. Recommending to use the same power supply to power V_{DD} and V_{DDA}, and the difference between V_{DD} and V_{DDA} should not exceed 300mV during power on normal operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.

5.3.2 Operating conditions at power-up / power-down

The parameters given in the table below are tested under general operating conditions.

Table 5.5 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions(1)	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	VCC=5V	0.8	∞	μs/V
	V_{DD} fall time rate		20	∞	

1. Unless otherwise specified, V_{DD} = 3.3V/5V, T_A = -40 °C to 125 °C.

5.3.3 Embedded reset and power control block characteristics

The parameters given in the table are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 5.4 General operating conditions.

Table 5.6 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector for level selection	VCC_LVL[1:0] = 00(Rising)	2.29	2.32	2.33	V
		VCC_LVL[1:0] = 00(Falling)	2.08	2.08	2.12	
		VCC_LVL[1:0] = 01(Rising)	2.87	2.87	2.94	
		VCC_LVL[1:0] = 01(Falling)	2.70	2.71	2.74	
		VCC_LVL[1:0] = 10(Rising)	3.66	3.66	3.73	
		VCC_LVL[1:0] = 10(Falling)	3.47	3.5	3.53	
		VCC_LVL[1:0] = 11(Rising)	4.29	4.3	4.34	
		VCC_LVL[1:0] = 11(Falling)	4.06	4.06	4.13	
$V_{PVDhyst}$(2)	PVD hysteresis	VCC=5V	160	240	240	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Rising edge	1.8	1.95	2.15	V
		Falling edge	1.65	1.8	1.98	
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	150	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization	VCC=5V	1.14	2	4.4	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

5.3.4 Embedded reference voltage

The parameters given in the Table are derived from tests performed under the ambient temperature and VDD supply voltage conditions summarized in Table 5.4 General operating conditions.

Table 5.7 Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	-40 °C < TA < +125 °C, VDD = 3.3V/5V	1.19	1.2	1.24	V
$T_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	TA=25 °C, 3.3V≤VDD≤5V	0.142	-	48.8	us
V_{REFINT}(2)	Internal reference voltage spread over the temperature range	-40 °C < T_A < +125 °C, V_{DD} = 3.3V/5V	-	-	15	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{COEFF}(2)	Temperature coefficient	-40 °C < T_A < +125 °C	-	-	382	ppm/°C

1. The shortest sampling time is obtained by multiple loops in the application.
2. Guaranteed by design, not tested in production.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Figure 5.4.

Table 5.8 Maximum current consumption in hold mode, code runs from internal Ram or Flash

Symbol	Parameter	Conditions	f_{HCLK}	Min	Typ	Max @ T_A(1)			Unit
				T_A= -40°C	T_A= 25°C	85 °C	105 °C	125 °C	
I_{DD}	Supply current in Hold mode	-40 °C < T_A <+ 125 °C, V_{DD}=3.3V	32 KHz	2	2.3	5.5	10.5	19.5	uA
		-40 °C < T_A <+ 125 °C, V_{DD}=5V	32 KHz	2.3	2.6	6.1	11	20.5	

1. Guaranteed by design.

Table 5.9 Maximum current consumption in run mode, data processing code runs from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)	Unit
				T_A=125°C	
I_{DD}	Supply current in Run mode	VCC=3.3V, External clock(2), all peripherals enabled	42MHz	49.5	mA
		VCC=3.3V, External(2), all peripherals are not enabled	42MHz	20	
		VCC=5V, External clock(2), all peripherals enabled	42MHz	52.5	
		VCC=5V, External(2), all peripherals are not enabled	42MHz	24	

1. Based on comprehensive evaluation and tested in production.

Table 5.10 Typical and Maximum current consumption in sleep mode

Symbol	Parameter	Conditions		f_{HCLK} (LRC)	Min	Typ(1)	Max @ T_A			Unit
					-40°C	25°C	85°C	105°C	125°C	
I_{DD}	Supply current in	-40 °C < T_A < +125 °C, HRC oscillator on, LDO on	V_{DD} = 3.3V	32KHZ	142	155	175	191	225	uA
			V_{DD} = 5V		144	158	178	194	227	

Symbol	Parameter	Conditions		f_{HCLK} (LRC)	Min	Typ(1)	Max @ T_A			Unit
					-40°C	25°C	85°C	105°C	125°C	
	Sleep mode	-40 °C < T_A < +125 °C, HRC oscillator off, LDO on	V_{DD} = 3.3V	32KHZ	21	28	47	62	93	
			V_{DD} = 5V		22	30	49	63	94	
		-40 °C < T_A < +125 °C, HRC oscillator off, LDO off	V_{DD} = 3.3V	32KHZ	2.4	3	12	25	52	
			V_{DD} = 5V		2.7	3.5	12.7	26	53	

1. Typical values were measured at T_A = 25°C.
2. Guaranteed by design.

5.3.6 External clock source characteristics

Table 5.11 HSE oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-		8	40	MHz
RF	Feedback resistor	-	-	300	-	kΩ
C	Recommended load capacitance	-	12	-	18	pF
i2	HSE Drive current	V_{DD}=5V,40MHz		1.1		mA
gm	Oscillator transconductance	Startup	3.56	5.84	7.39	mA/V
tSU(HSE)	Startup time	V_{DD} is stabilized, 40MHz	-	1.4	-	ms

5.3.7 Internal clock source characteristics

Table 5.12 High speed interior oscillator (HRC) characteristics(1)

Symbol	Description	Conditions		Min	Typ	Max	Unit
f_{HRC}	frequency	-		-	42	-	MHz
$Duty_{(HRC)}$	Duty cycle	-		45	-	55	%
ACC_{HRC}	HRC oscillator accuracy	User can adjust the HRCADJ register(2)		-	-	±1 (2)	
		Factory calibration(4)	T_A = -40 to 125 °C	-3.9	-	2.3	
$t_{su(HRC)}$(4)	HRC oscillator Startup time	-			10		µs
$I_{DD(HRC)}$(4)	HRC oscillator consumption	-			91	120	µA

1. Unless otherwise specified, V_{DD} = 3.3V, T_A = -40 to 105°C.
2. Refer to the reference manual.

3. Guaranteed by design.
4. Guaranteed by comprehensive evaluation.

Table 5.13 Low speed interior oscillator (LRC) characteristics(1)

Symbol	Description	Min	Typ	Max	Unit
f_{LRC}(2)	frequency	23	32	42	kHz
$t_{su(LRC)}$(3)	LRC oscillator Startup time		70		μs
$I_{DD(LRC)}$(3)	LRC oscillator consumption		0.3		μA

1. Unless otherwise specified, V_{DD} = 3.3V, T_A = -40 to 85°C.
2. Guaranteed by design.
3. Guaranteed by comprehensive evaluation.

Wake-up time from low power mode

The wake-up times in the following table are measured using the HRC as the clock source. In practice, the clock source after the chip is woken up is related to the current operation mode:

Sleep mode: the clock source is the clock that was set before entering Sleep mode.

Hold mode: clock source is HRC.

Table 5.14 Wake-up time on low power mode

Symbol	Description	Conditions	Typical value	Unit
t_{WUHOLD} (1)	Wake up from hold mode, F_{sys}=HRC	VCC=3.3V	2.08	ms
		VCC=5V	2.08	
	Wake up from hold mode, F_{sys}=LRC	VCC=3.3V	11.55	
		VCC=5V	11.55	
$t_{WUSLEEP}$(1)	Wake up from sleep mode, F_{sys}=HRC	VCC=3.3V	2.2	μs
		VCC=5V	2.2	
	Wake up from sleep mode, F_{sys}=LRC	VCC=3.3V	2.18	
		VCC=5V	2.17	

1. Wake-up time is measured from the wake-up event until the user program reads the first instruction.

5.3.8 Memory characteristics

Table 5.15 Flash characteristics

Symbol	Parameter Description		Min(1)	Typ	Max(1)	Unit
FlashSize	Flash Space Size		-	32	-	kbytes
InfoSize	Information Block Space Size		-	2	-	kbytes
RamSize	Ram Space Size		-	4	-	kbytes
Tflashrd	Flash Byte Read Time		-	-	40	ns
Tflashwr	Flash Byte Write Time		20	-	-	us
Tflashper	Flash Page Erase Time		2	-	-	ms
Tflashmer	Flash Full Erase Time		10	-	-	ms
FPageSize	Code Flash Page Size		-	1	-	kbytes/page
InPageSize	Information Block Page Size		-	2	-	kbytes/page

Symbol	Parameter Description		Min(1)	Typ	Max(1)	Unit
Tdat	Data Retention Time		10	-	-	years
Tmprun	Operation temperature	Numwr(2) = 100K	-40	-	85	°C
		Numwr(2) = 10K	-40	-	105	°C
Vram	RAM Data hold voltage		-	1.35	-	V

1. Guaranteed by design.
2. Erase and Write number

5.3.9 EMC characteristics

Table 5.16 EMS characteristics

Symbol	Description	Conditions	Max absolute value
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 5V, T_A = +25 °C, f_{HCLK} = 42MHz. Discharging of air.	±4000V
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 5V, T_A = +25 °C, f_{HCLK} = 42MHz. Conforming to IEC 61000-4-2	±2500V

5.3.10 Electrical sensitivity characteristics

Table 5.17 ESD absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JEDEC EIA/ JESD22-A114	±2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JEDEC JS-002-2018	±1200	

Table 5.18 Electrical sensitivities

Symbol	Parameter	Conditions	Maximum value	Unit
LU	Static latch-up class	T_A = +125 °C, conforming to JEDEC 78E	±200	mA

5.3.11 IO port characteristics

Table 5.19 IO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard I/O pins, Low level input voltage	-	-	-	0.13*VDD+0.4	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Standard I/O pins, High level input voltage	-	0.6*VDD+0.13	-	-	
V_{hys}	Standard I/O Schmitt trigger hysteresis (1)	V_{DD} = 3.3V	1.1		1.3	V
		V_{DD} = 5V	1.6		1.9	V
I_{lkg}	Input leakage current(3)	V_{IN}=V_{DD}	-	-	±1	μA
		V_{IN}=0	-	-	±1	
R_{PU}	Weak pull-up equivalent resistor (4)	V_{DD}=3.3V	55	85	135	kΩ
		V_{DD}=5V	33	48	75	
R_{PD}	Weak pull-down equivalent resistor (4)	V_{DD}=3.3V	30	50	95	
		V_{DD}=5V	20	32	55	
C_{IO}	I/O pin capacitance	-	-	7	-	pF

1. Hysteresis voltage at switching level of Schmidt trigger. Guaranteed by comprehensive evaluation, not tested in production
2. At least 100mV.
3. If there is reverse current backflow at adjacent pins, the leakage current may be higher than the maximum value.
4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

Table 5.20 Output voltage characteristics

Symbol	Description	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage, when 1 pin absorbs current at the same time	V_{DD}=3.3V,I_{io}=8mA	-	0.1	V
		V_{DD}=5V,I_{io}=10mA	-	0.3	
V_{OH}(2)	Output high level voltage, when 1 pin putput current at the same time	V_{DD}=3.3V,I_{io}=8mA	2.67	-	
		V_{DD}=5V,I_{io}=10mA	4.5	-	
I_{source}	When V_{io}=0.9V_{DD}, IO push-pull outputs a high level	V_{DD}=3.3V	4.4	4.5	mA
		V_{DD}=5V	8.9	9.1	
I_{sunk}	When V_{io}=0.1V_{DD}, IO push-pull outputs a low level	V_{DD}=3.3V	6.9	7	
		V_{DD}=5V	13.8	13.9	

1. The current I_{IO} absorbed by the chip must always follow the absolute maximum rating given in the current characteristic table.
2. The current I_{IO} at the chip output must always follow the absolute maximum rating given in the current characteristic table, while the sum of I_{IO} (all I/O pins and control pins) must not exceed the I_{VDD}.
3. Guaranteed by comprehensive evaluation.

Table 5.21 IO AC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{max(IO)out}$	Maximum frequency	No load, V_{DD}=3.3V	-		21	MHz
		No load, V_{DD}=5V	-		21	
		C_L = 10 pF, V_{DD} = 3.3V	-		20	
		C_L = 10 pF, V_{DD} = 5V	-		21	
$t_{f(IO)out}$	Output drop time from high to low level	C_L = 10pF, V_{DD} = 3.3V	-		12	ns
		C_L = 10 pF, V_{DD} = 5V	-		9	
$t_{r(IO)out}$	Output rise time from	C_L = 10pF, V_{DD} = 3.3V	-		11	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	high to low level	C_L = 10 pF, V_{DD} = 5V	-		9	
t_{EXTIpw}	EXTI controller detects the pulse width of the external signal	VCC=3.3V, Turn on filter 50ns	-	50	55	ns
		VCC=3.3V, Turn on filter 80ns	-	80	88	
		VCC=5V, Turn on filter 50ns	-	50	56	
		VCC=5V, Turn on filter 80ns	-	80	91	

5.3.12 NRST pin characteristics

Table 5.22 NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	V_{DD}=3.3V	-	-	0.9	V
		V_{DD}=5V	-	-	1.2	
$V_{IH(NRST)}$(1)	NRST input high level voltage	V_{DD}=3.3V	2.52	-	3.6	
		V_{DD}=5V	3.91	-	5.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis (2)	V_{DD}=3.3V	-	1.72	-	
		V_{DD}=5V	-	2.73	-	
R_{PU}	Weak pull-up equivalent resistor	-	-	10	-	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	V_{DD}=3.3V	-	1.8	-	us
		V_{DD}=5V	-	1.1	-	
$V_{NF\ (NRST)}$(1)	NRST input not filtered pulse	V_{DD}=3.3V	-	1.9	-	
			-	1.2	-	

1. Guaranteed by design.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).

5.3.13 Timer characteristics

Table 5.23 TIMx characteristics

Symbol	Description	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 42 MHz	23.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 42 MHz	0	21	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{counter}$	16-bit counter clock cycles when an internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 42 MHz	0.0238	1560	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 42 MHz	-	102.2	s

1. TIMx is a generic name that stands for TIM0~ TIM3 and TIM8.

5.3.14 Communication interfaces

I2C interface characteristics

Table 5.24 I2C interface characteristics

Symbol	Description	Min	Max	Unit
$t_{w(SCLL)}$	SCL low level width	4.7	-	μs
$t_{w(SCLH)}$	SCL high level width	4	-	
$t_{su(SDA)}$	SDA setup time	250	-	μs
$t_{h(SDA)}$	SDA data holding time	-	3450(2)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL drop time	-	300	
$t_{h(STA)}$	start condition holding time	4	-	μs
$t_{su(STA)}$	repeat starting condition establishment	4.7	-	
$t_{su(STO)}$	stop condition establishment time	4	-	μs
$t_{w(STO:STA)}$	stop to start condition time	4.7	-	μs
C_b	single bus load capacitance	-	400	pF

1. Standard I2C mode.
2. Must ensuring the SDA maintains a stable level in the SCL high level interval.

Table 5.25 SCL frequency（f_{PCLK1} = 36MHz，V_{DD_I2C} = 3.3V/5V）

f_{SCL}(KHz)	I2CCON_CR[9:0] value
	R_P = 4.7 kΩ
400	0x019
300	0x022
200	0x033
100	0x068
50	0x0d1
20	0x20c

1. RP = External pull-up resistor，f_{SCL} = I2C speed.
2. For speeds around 200KHZ, the achieved speed tolerance bit is ±5%. For the other speed ranges, the speed tolerance is ±2%. This variable depends on the accuracy of the external components adopted at the time of application design.

5.3.15 ADC characteristics

Table 5.26 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	2.5	-	5.5	V
V_{REF+}	Positive reference voltage	-	-	V_{DDA}	-	V
f_{ADC}	ADC clock frequency	-	0.5	-	14	MHz
fs(2)	Sampling rate	-	0.036	-	1	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14MHz	-	-	700	kHz
			-	-	20	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	V_{DD}=3.3- 5V	1	-	1.05	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	10	-	pF
t_{latr}(2)	Normal trigger conversion latency	f_{ADC} = 14 MHz			0.143	μs
		-			2	$1/f_{ADC}$
t_s(2)	Sampling time	General purpose channel	2	-	256	$1/f_{ADC}$
t_{STAB}(2)	Stabilization time	-	-	-	1	μs
t_{CONV}(2)	Total conversion time (including sampling time)	-	-	-	12	μs
						$1/f_{ADC}$

1. Guaranteed by comprehensive evaluation, not tested in production.
2. Guaranteed by design.
3. In the partial pin package, V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. For external triggering, a delay $1/f_{PCLK2}$ must be added to the delay listed in the above table.

Table 5.27 R_{AIN} max for f_{ADC} = 14MHz

T_s (cycles)	t_s (μs)	R_{AIN} max (kΩ)
2	0.142	0.4
4	0.284	0.75
8	0.568	1.6
16	1.136	3.1
32	2.272	6.5
64	4.544	13
128	9.088	25.5
256	18.175	50

Table 5.28 ADC accuracy – limit test conditions

Symbol	Parameter	Conditions	Typ	Unit
ET	Total unadjusted error	f_{sys}=42MHz, f_{ADC} = 14 MHz, RAIN < 10 kΩ, V_{DDA} = 3.3 to 5V, T_A = 25 °C, Measurements were made after the ADC calibration.	±25	LSB
EO	Offset error		15	
EG	Gain error		5	
ED	Differential linearity error		±2	
EL	Integral linearity error		±5.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
3. Guaranteed by design.

5.3.16 PGA characteristics

Table 5.29 PGA characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Supply voltage	-	2.5	3.3.	5.5	V
CMIR	Common mode input range	-	0	-	V_{DDA}	V
R_{INDIF}	Differential input impedance	-	1	-	24.5	KΩ
ICC	Operation current	Unit gain circuit, VCC=3.3V	-	470	720	uA
		Unit gain circuit, VCC=5V	-	610	930	
V_{OLR}	Output range	-	V_{SS}+0.2	-	V_{DD}-0.2	V
PGA gain error	PGA gain error	2 x Gain	-2	-	2	%
		4 x Gain	-4	-	4	
		8 x Gain	-4	-	6	
TST(1)	Stability time	1% difference from the final value（CLOAD=10pF）	116	142	179	ns
Av	Magnification factor	-	-	2	-	V/V
			-	4	-	
			-	8	-	

1. Guaranteed by design.

5.3.17 CMP characteristics

Table 5.30 CMP characteristics

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.5	3.3	5.5	V
V_{IN}	Comparator input voltage range	-	0	-	V_{DDA}	
t_{START}	Comparator startup time to reach propagation delay specification	-	-	-	10	us
t_D(4)	Response time: (VDD = 3.3V; N-terminal level is 1.65V, P-terminal level overshoots 100Mv with N-terminus)	High speed mode	-	100	170	ns
		Medium speed mode	-	175	216	
		Low speed mode	-	320	308	
		Very Low speed mode	-	594	1050	
V_{offset}(3)	Comparator offset error	Full V_{DDA} voltage range, full temperature range	-	-	±10	mV
V_{hys}	Comparator hysteresis	CR1_HYST=00	-	0	-	mV
		CR1_HYST=01	4.74	5	7.01	

Symbol	Description	Conditions	Min	Typ	Max	Unit
		CR1_HYST=10	9.25	10	13.8	
		CR1_HYST=11	14.2	20	25.6	
I_{CC}	Operation current	VDD=3.3V, Very Low rate	-	26	-	uA
		VDD=3.3V, low rate	-	38	-	
		VDD=3.3V, medium rate	-	60	-	
		VDD=3.3V, High rate	-	100	-	

1. Guaranteed by design.
2. Refer to the table for internal reference voltage.
3. Guaranteed by comprehensive evaluation.
4. The typical value is the average of all comparator propagation delays.

5.3.18 VDD15

Table 5.31 VDD15 characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD15}	-	-40℃<T_A<+125℃, V_{DD}=3.3V		1.5		V
		-40℃<T_A<+125℃, V_{DD}=5V		1.5		
V_{DD}	Supply voltage		2	5	5.5	V
I_{VDD}	Static power consumption	PVT	7.3	14	45	uA
V_{OUT}	Output voltage		1.47	1.5	1.52	V
I_{OUT}	Drive capability	V_{DD}>2.4V			40	mA
		2V<V_{DD}<2.4V			20	
C_{LOAD}	Load Capacitance		0.47	0.47	4.7	uF
Load regulation		Load from 100nA to 40mA	0.26	865	1360	mv/A
Line regulation			11		19	mV

6 Gate driver

6.1 Operating Conditions

Table 6.1 Gatedriver absolute maximum ratings

Symbol	Description	Min	Max	Unit
V_{vin}	Bus Voltage Input Voltage	-0.3	28	V
V_{LDO}	5V LDO Output Voltage	-0.3	5.5	
$V_{HIN1,2,3}$	High-side Control Terminal Input Voltage	-0.3	5.5	
$V_{LIN1,2,3}$	Low-side Control Terminal Input Voltage	-0.3	5.5	
$V_{HO1,2,3}$	High-side driver outputs	-0.3	V_{vin}	
$V_{LO1,2,3}$	Low-side driver outputs	-0.3	$V_{LIN1,2,3}$	
PD	Power Consumption	-	0.5	W
R_{thJA}	Thermal Resistance	-	125	°C/W
TJ	Junction Temperature	-40	150	°C
TS	Storage Temperature	-55	150	
V_{ESD}	ESD	2		KV

Table 6.2 Gatedriver recommended operating conditions

Symbol	Description	Min	Max	Unit
V_{vin}	Bus Voltage Input Voltage	10	28	V
$V_{HIN1,2,3}$	High-side Control Terminal Input Voltage	0	5	V
$V_{LIN1,2,3}$	Low-side Control Terminal Input Voltage	0	5	V
$V_{HO1,2,3}$	High-side driver outputs	6.5	V_{vin}	V
$V_{LO1,2,3}$	Low-side driver outputs	0	5	V
F_{PWM}	PWM Switching Frequency 1nF	-	50	KHz

6.1 Electrical Characteristics

6.1.1 Dynamic Electrical Characteristics

The dynamic characteristics of the gate driver are shown in the figure below.

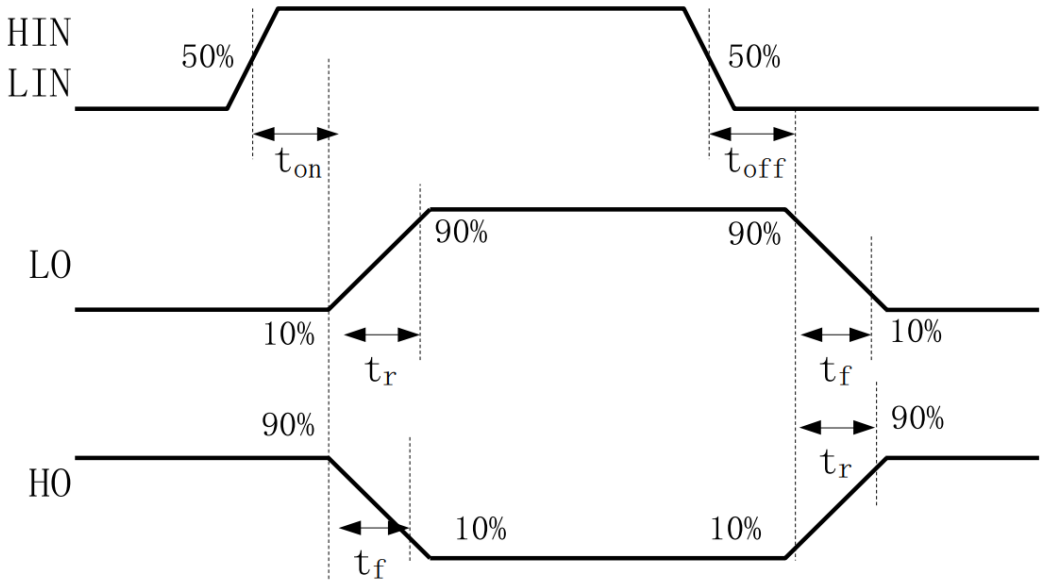


Figure 6.1 Timing Switching Waveform Diagram

(VCC= 24V, CL = 1nF, TA= 25°C)

Table 6.3 Dynamic Electrical Characteristics of Gatedriver

Symbol	Description	Conditions	Min	Typ	Max	Unit
TON	Turn-on Delay Time		-	80	150	ns
TOFF	Turn-off Delay Time		-	80	150	
THR	HO Rise Time		-	100	500	
THF	HO Fall Time		-	150	500	

6.1.2 Static Electrical Characteristics

(VCC= 24V, CL = 1nF, TA= 25°C)

Table 6.4 Static Electrical Characteristics of Gatedriver

Symbol	Description	Conditions	Min	Typ	Max	Unit
IQCC	VCC Quiescent Current	HIN=LIN=0V	0.3	0.5	1.0	mA
VDD	VDD Output Voltage		4.3	-	5.5	V
VIH	Logic "1" Input Voltage		2.2	-	-	V
VIL	Logic "0" Input Voltage		-	-	0.6	V
VHO	HO Output Voltage	HIN=5V	VCC-11.5	VCC-10	VCC-8.5	V
		10V< VCC <14V	6.5		-	V

(VCC= 24V，CL = 1nF，TA= 25°C)

Table 6.5 Driving NMOS Power Transistor

Symbol	Min	Typ	Max	Unit
Input Resistance	40	50	60	Ω
Pull-down Resistance	16	20	24	KΩ

7 Package information

7.1 TSSOP28 package information

TSSOP28 is 28-pin, 9.7 * 4.4mm low-profile quad flat package.

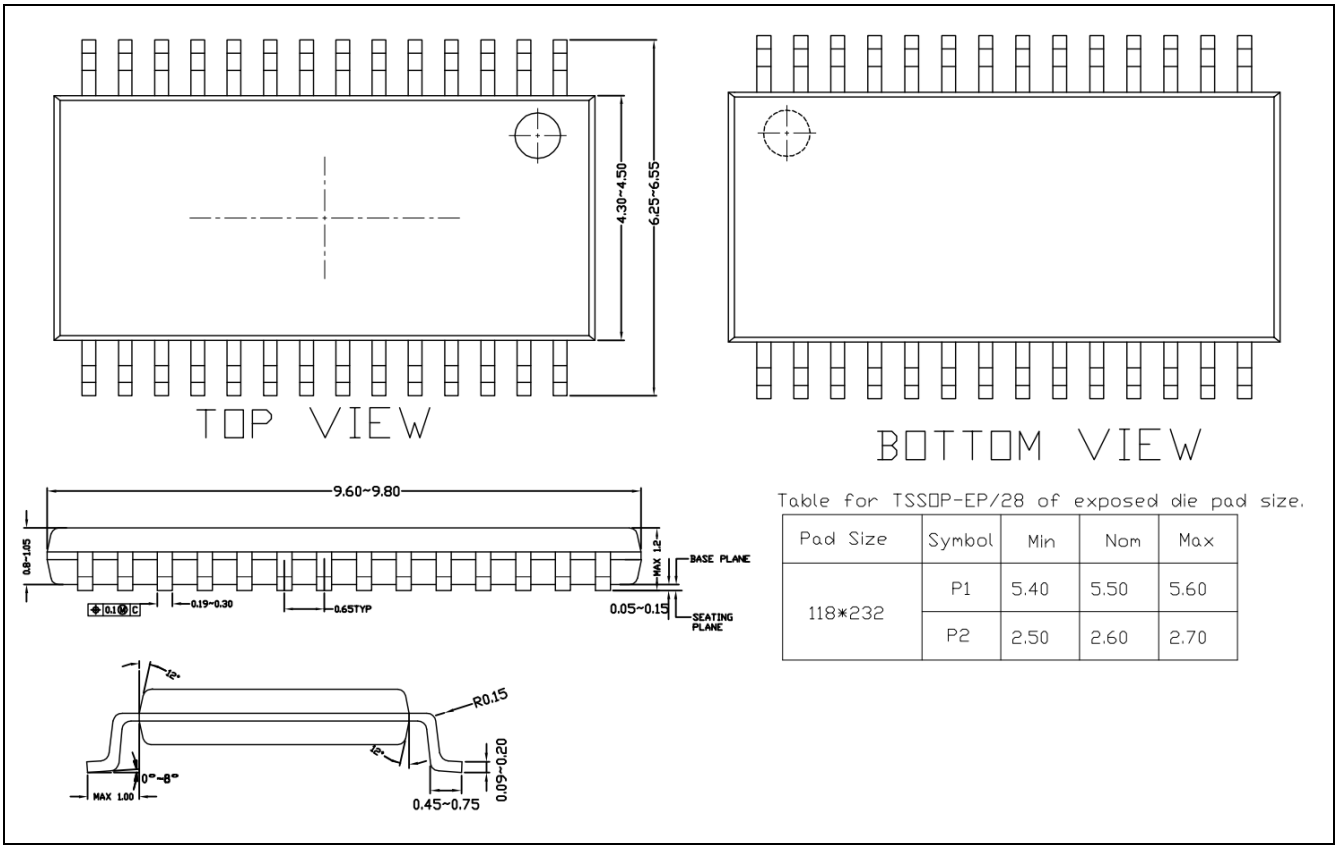


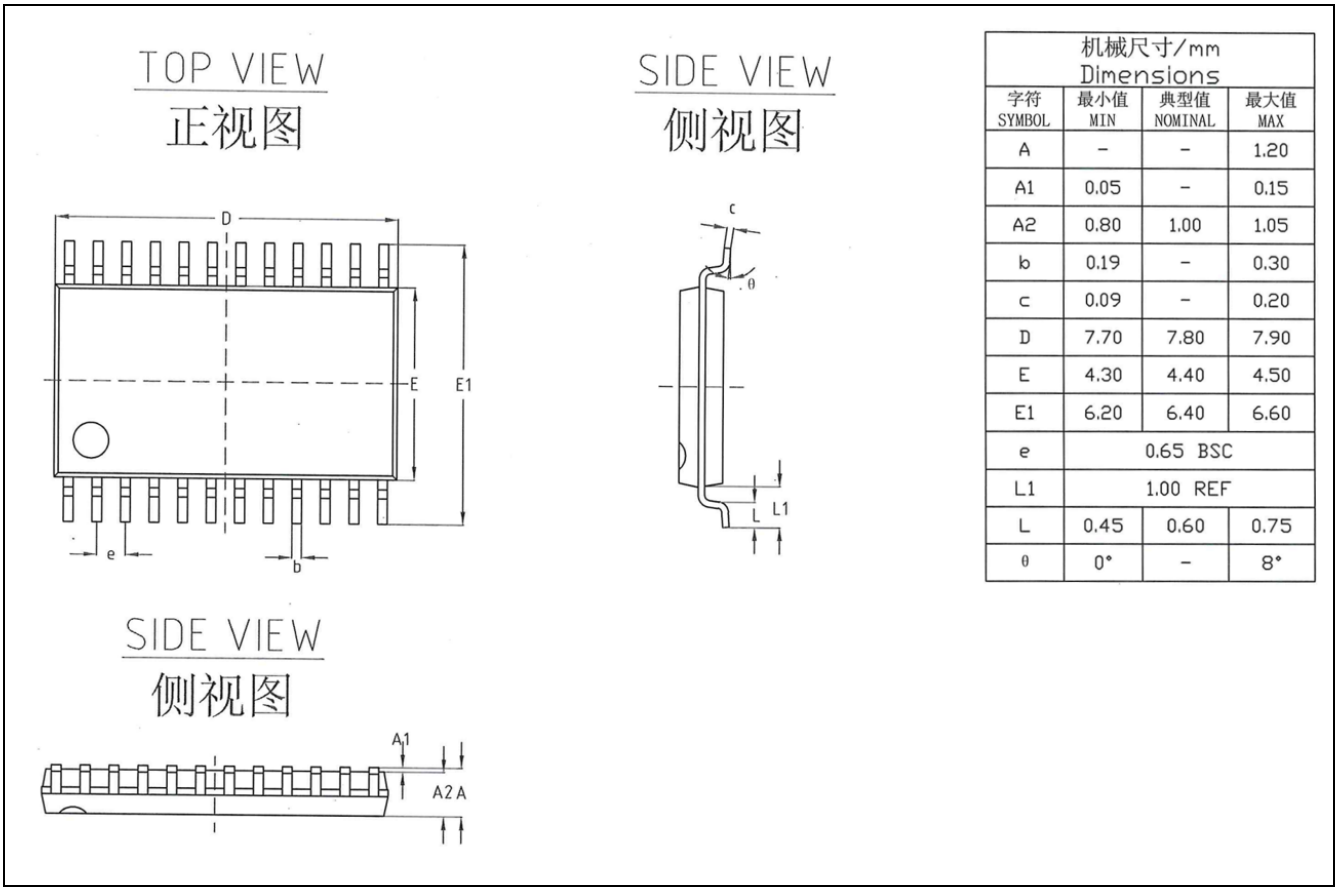
Figure 7.1 TSSOP28 package outline

Table 7. 1 TSSOP-EP/28 of exposed die pad size

Pad Size	Symbol	Min	Nom	Max
118*232	P1	5.40	5.50	5.60
	P2	2.50	2.60	2.70

7.1 TSSOP24 package information

TSSOP24 is 24-pin, 7.8 * 4.4mm low-profile quad flat package.



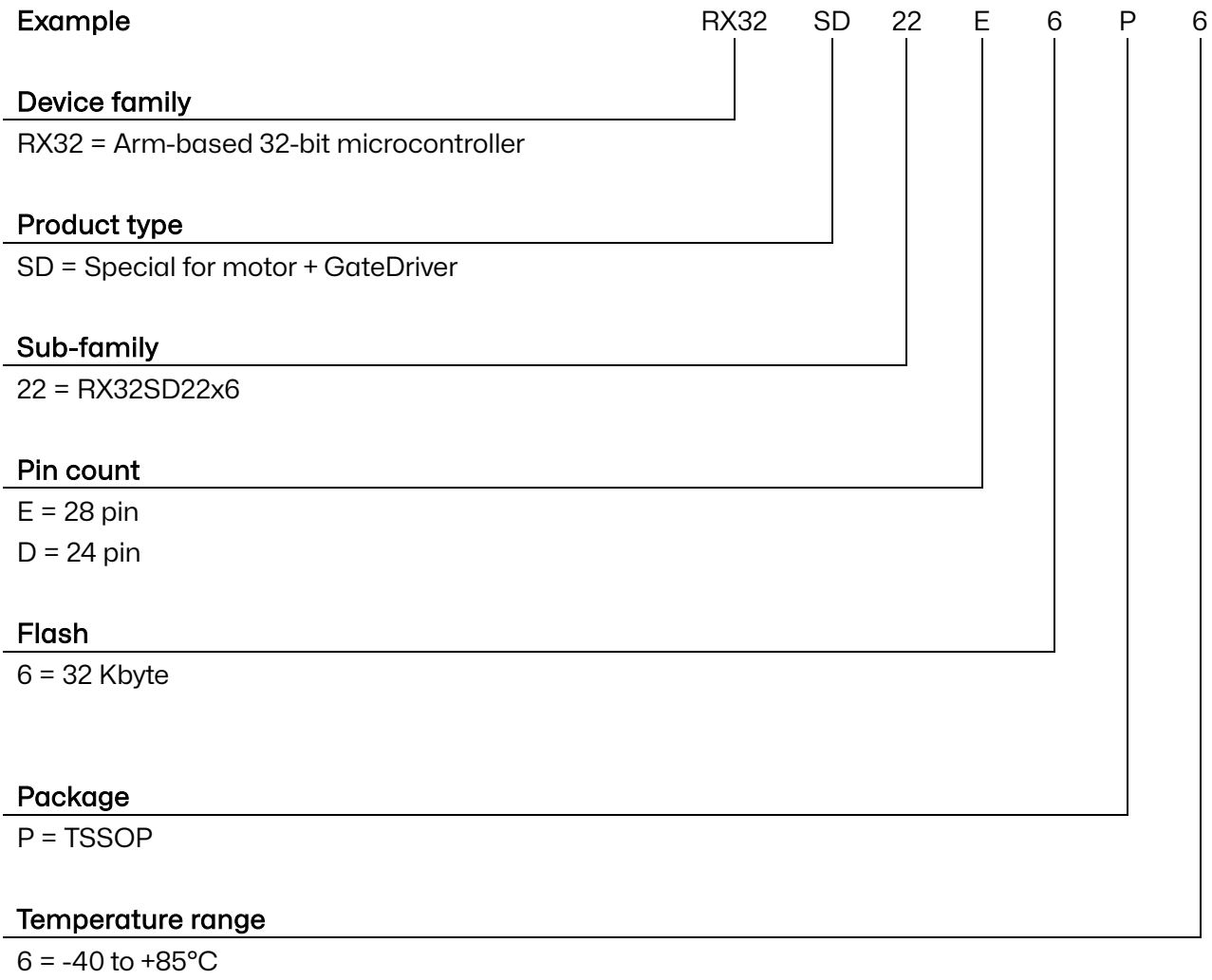
机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	7.70	7.80	7.90
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
θ	0°	-	8°

Figure 7.2 TSSOP24 package outline

Table 7. 2 TSSOP24 mechanical data/mm

Symbol	Min	Nom	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	7.70	7.80	7.90
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
θ	0°	-	8°

8 Ordering information



9 Revision history

Table 9.1 Document revision history

Date	Revision	Changes
2023/8/7	V2.0	1. New edition
2023/9/20	V2.1	1. RX32SD22 Architecture Diagram ME part data update 2. Unify the concepts of HSI and LSI 3. Update of power supply scheme block diagram 4. Ordering information Chip Sub-family name update 5. Addition of a pin definition table
2023/11/8	V2.2	1. Improved the formatting of some tables 2. Corrected a typo in Table 5.18 3. HSI revise to HRC, LSI revise to LRC 4. Revise Alternate function Table 5. SDK Libraries V1.5 Low-power modes corresponds to this new version of Data Sheet, the old version of SDK Libraries V1.4 and the previous version correspond to the old version of Data Sheet.
2024/8/23	V2.3	1. Increased Flash specifications, operating temperature -40~105°C with 10K erase and write cycles. 2. Revised chip operating temperature to -40~105°C. 3. Revised chip ambient temperature to -40~105°C. 4. Revised chip junction temperature range to -40~150°C.
2025/4/15	V2.4	5. Update $V_{ESD(HBM)}$ to 2000V.